

FIG.1

Aquaia --- HdCd.appt

File Edit View Run Wizards Help

Template title: 10S latest SILK

Parameter	Value
MCBAR	
CA	
M1	
V1	
M2	
V2	
M3	
V3	
M4	
V4	
M5	
V5	
M6	
VL	
MJ	
VJ	
MK	
VK	
MP	
va	

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FIG.2A

FIG.2B

Aquaia - - - HdCd.aprt

File Edit View Run Wizards Help

Template title : 10S latest SILK

Parameter	Value
[-] ... M2	
[-] ... General	
[-] ... Technology parameters	
... Total thickness	0.25
... Minimum Width	0.315
... Minimum Space	0.315
... Signal line width	0.1
... Signal line space	0.1
... Taper angle from horizontal	90
... Line width measure at (% wire thickness from bottom)	100
... Effective resistivity	2.2
... k of medium between wires	2.65
... Is there a cap ?	Yes
... Cap thickness	0.05
... k of cap	4.5
... Is there a hard mask ?	Yes
... Hard mask thickness	0.025
... k of hard mask	4.5
... Is there RIE stopper ?	NO
[-] ... Template parameters	

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FIG.3A

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Calculate 2D capacitances

Variables

Calculation options

Variable choices

Calculate for several layers using default values

Specify signal wire layer and set variables

Signal wire in layer : M4

Variable in layer : M4

Parameter : Signal line space

Single value

List (comma separated)

Range

From: 0.1

To:

Step:

Keep pitch constant

Vary width and space by the ratio

Treat width and space as independent

Layer list

M3

M4

MJ

Variable List

M4 Signal line width 0.45

Add

Remove

Variation choices

Treat variables as independent

Vary simultaneously

Simulate full matrix

Help

Start

Cancel

Calculate 3D capacitances

Variables **Calculation options**

Variable choices

☒ Calculate for several layers using default values

☒ Specify signal wire layer and set variables

Signal wire in layer :

No. of layers above signal layer to consider

Orthogonal loading density above (%)

No. of layers below signal layer to consider

Orthogonal loading density below (%)

Variable in layer :

Parameter :

☒ Single value

☐ List (comma separated)

☐ Range

From: To: Step:

☒ Keep pitch constant

☐ Vary width and space by the ratio

☐ Treat width and space as independent

Layer list

B2	▲
FW	
FL	▼

Variable List

M3 Signal line width 0.25

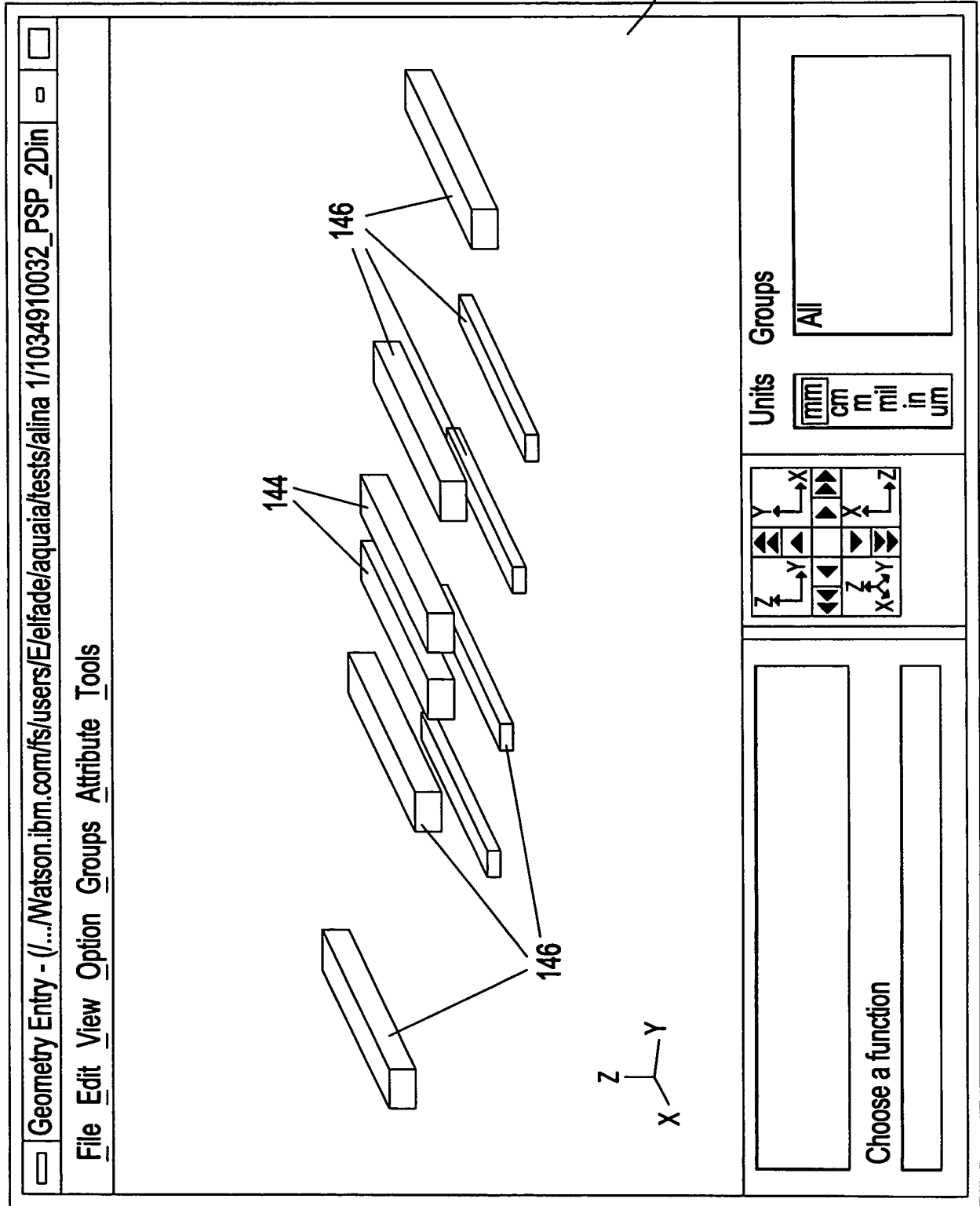
Variation choices

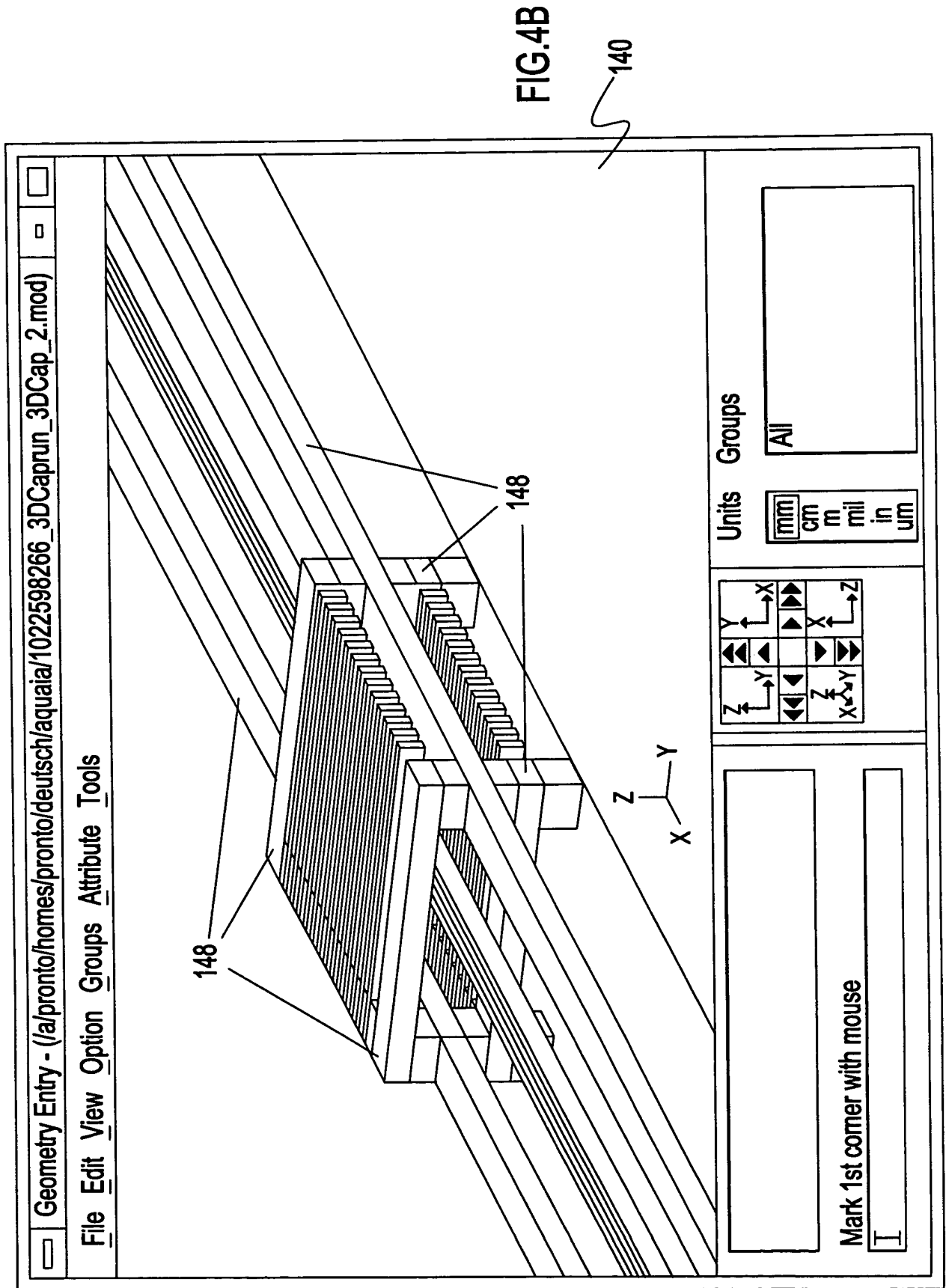
☒ Treat variables as independent

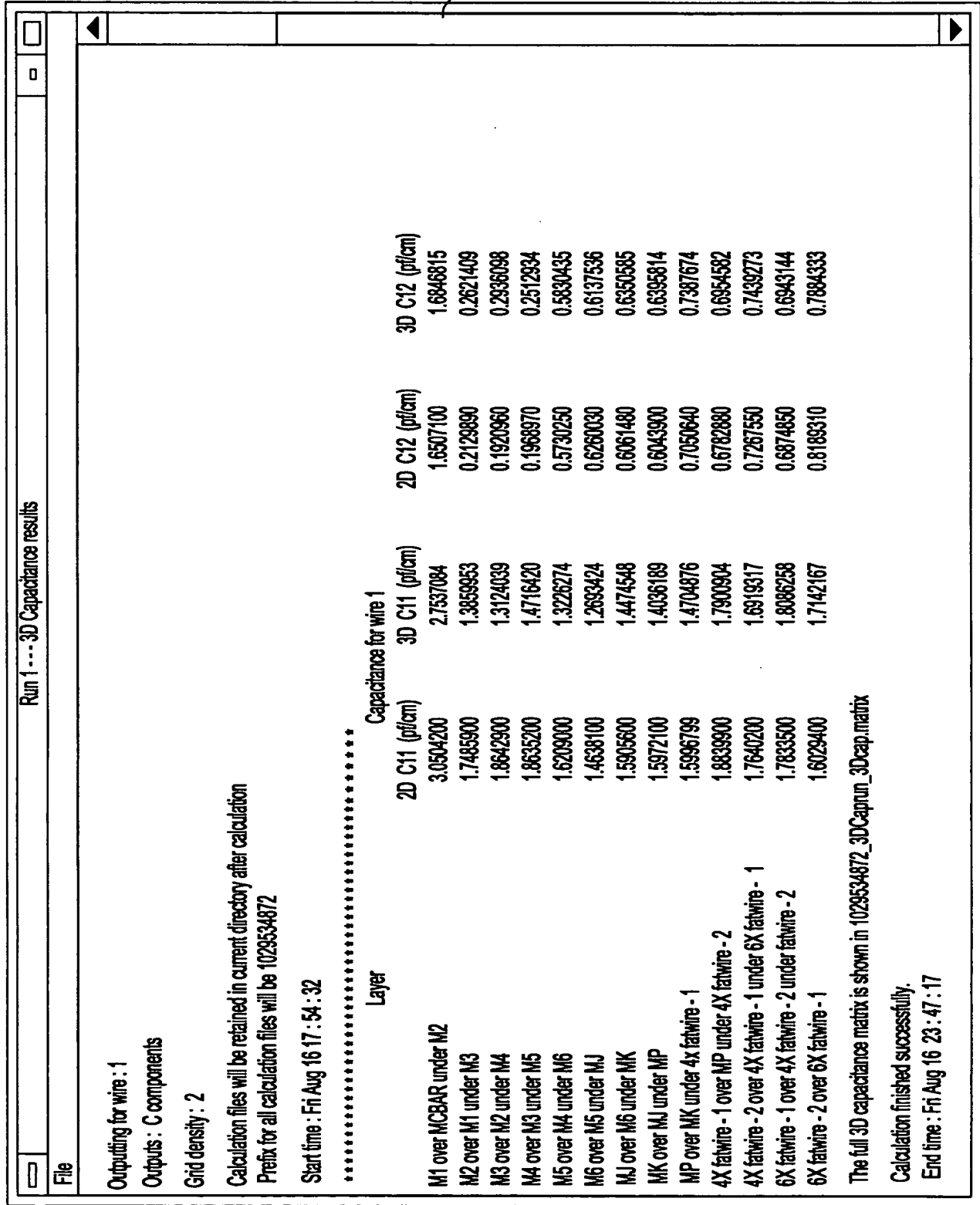
☐ Vary simultaneously

☐ Simulate full matrix

FIG.3B







PowerSpice Simulation			
Layer Template Variables	Circuit Variables	Output and Model Options	
Variables and values			
Select circuit variables			
Single value	2.5		
List (comma separated)			
Range			
From:		To:	Step:
Select device technology :		cmos9s t002	
Circuit Variable List			
Input buffer NFET width (um) 2			
Driver NFET width (um) 24			
Wire length (um) 2000			
Load NFET width (um) 2			
Next stage driver NFET width (um)			
Beta ratio 2.5			
		Set	Remove
Temporary files			
Temporary file directory		Browse	
Delete calculation files			
Retain files			
Help		Start	Cancel

FIG.5A

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FIG.5B

PowerSpice Simulation

Layer Template Variables | Circuit Variables | **Output and Model Options**

Output options

- ☐ Output driver delay
- ☐ Output wire delay
- ☐ Output load delay
- ☐ Output rise/falltime at driver input
- ☐ Output rise/falltime at near end
- ☐ Output propagated rise/falltime
- ☒ Output F EN
- ☐ Output N EN

Frequency-independent model options

- ☐ R2dC model
- ☐ R2dL2dC model
- ☐ R2dL3dC model
- ☐ R3dC model
- ☐ R3dL3dC model

Frequency-dependent model options

- ☒ 2dR(f)2dL(f)2dC model
- ☐ 2dR(f)2dL(f)3dC model
- ☐ 2dR(f)3dL(f)3dC model

TL algorithm options

- ☐ RLINE
- ☒ OMRA
- ☒ SYNTH

PowerSpice model files

PowerSpice model file directory .

☐ Delete PowerSpice model files

☒ Retain PowerSpice model files

Switching configuration

No. of signal wires: 3

Delay/risetime :

Crosstalk :

PowerSpice model file directory . **Browse**

Help **Start** **Cancel**

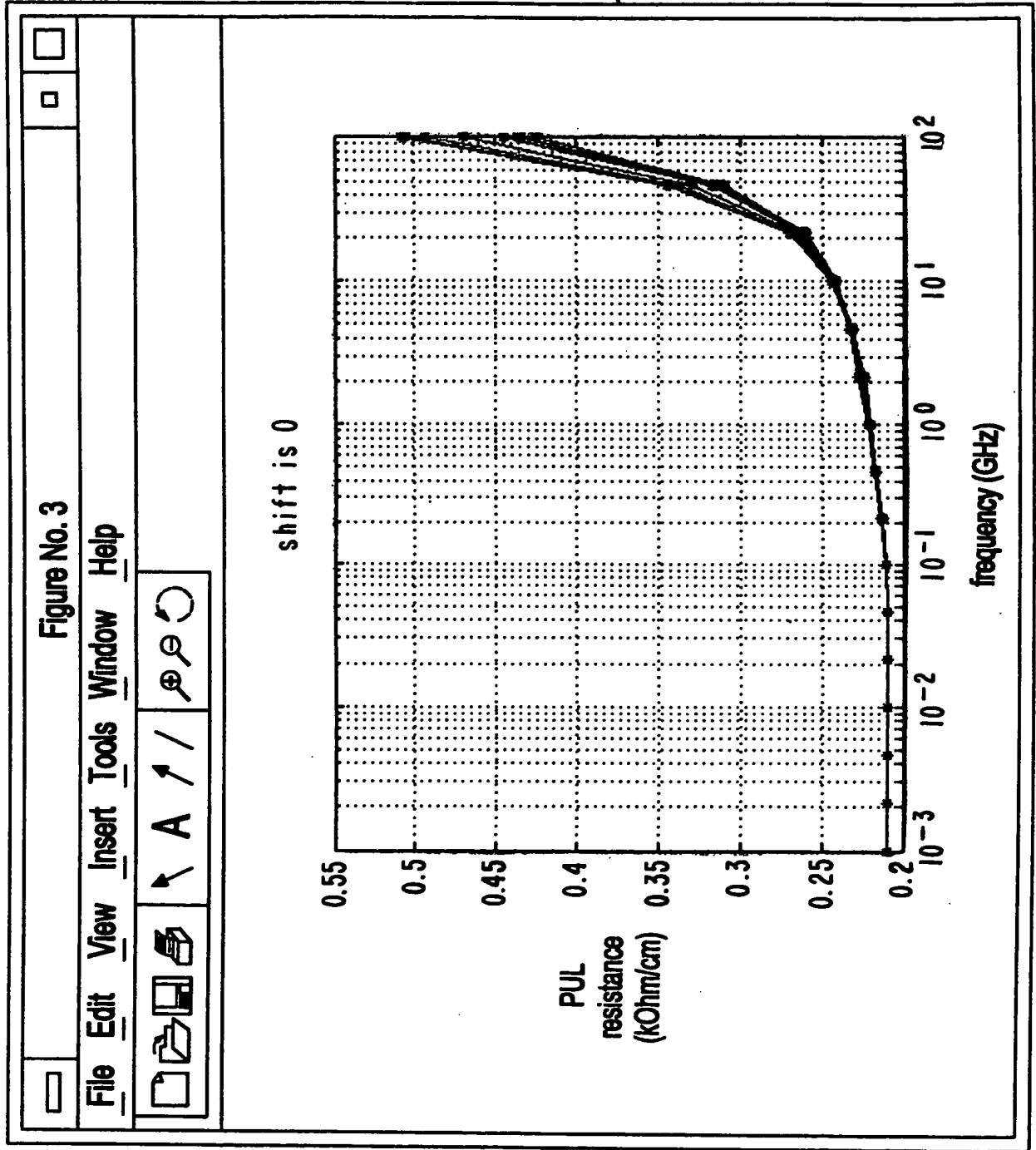


FIG.6A

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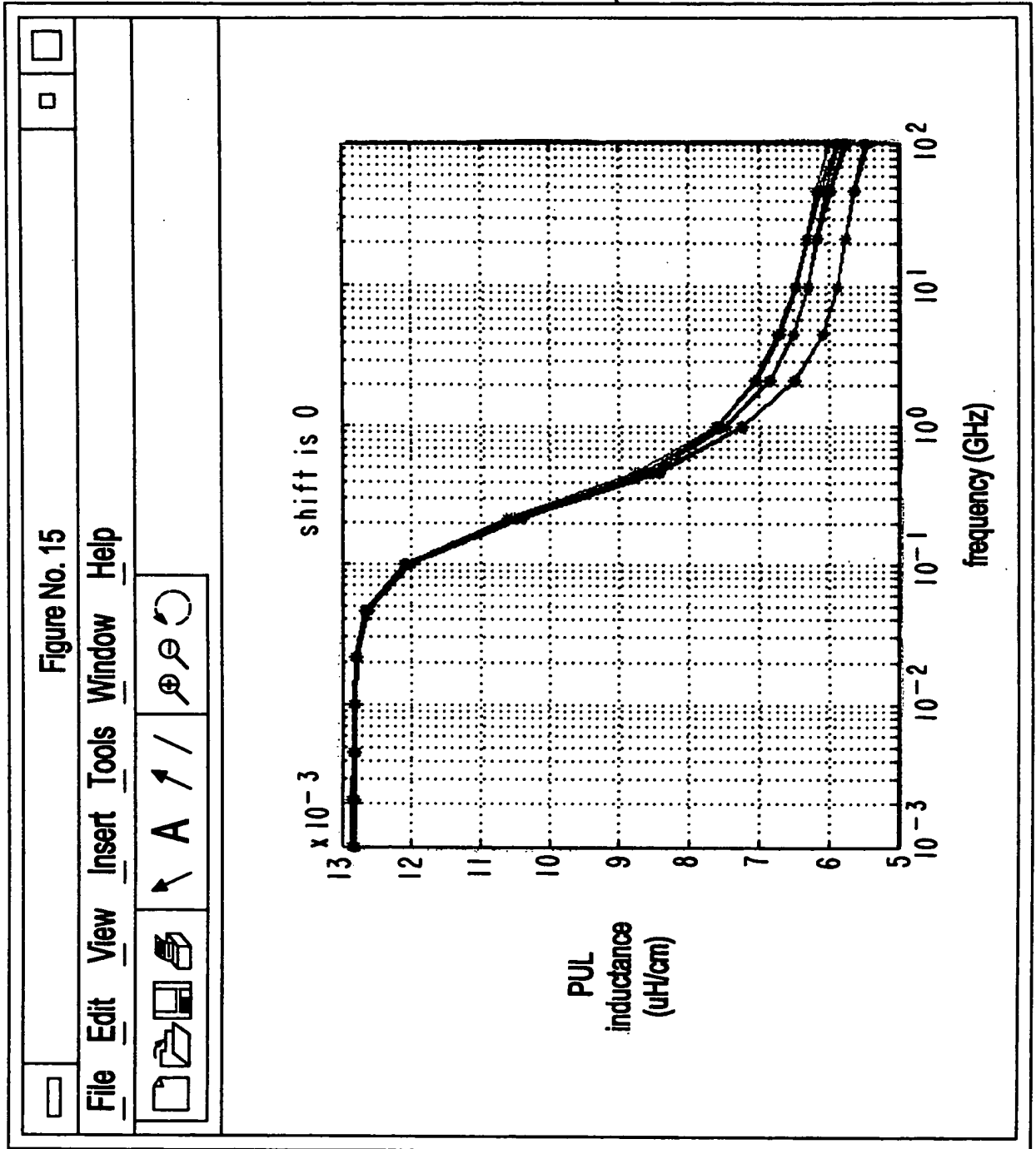


FIG.6B

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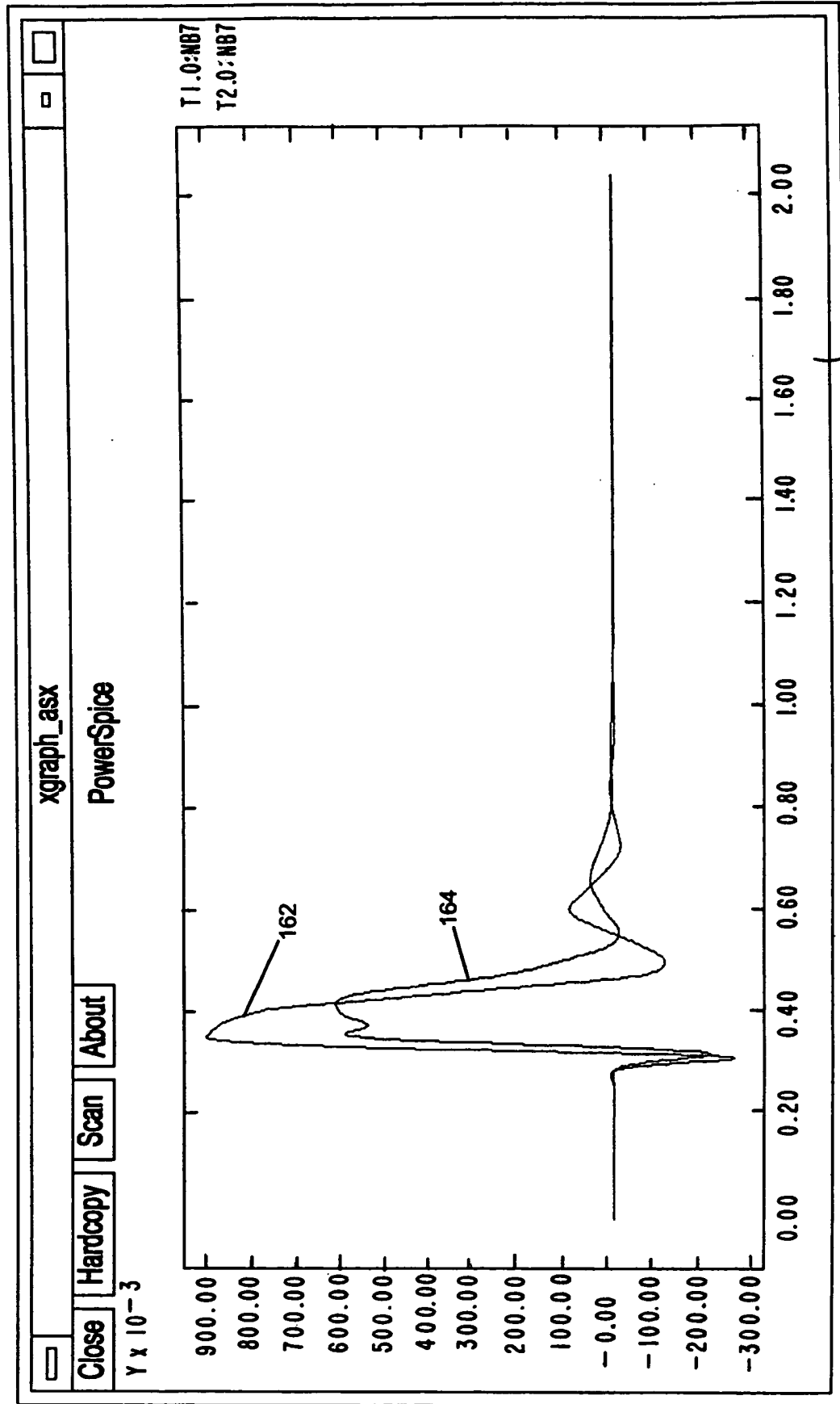


FIG.7